

WE CLAIM:

1. A peak power regulator, input with at least one input signal, that outputs at least one output signal corresponding to the input signal, the power regulator
5 comprising:

first and second delay apparatus that generate first and second delayed signals corresponding to the input signal;

a power estimation apparatus that generates, with
10 use of the input signal, an overall input power estimation signal corresponding to the input signal;

a scaling factor generator that generates a scaling factor with use of the overall input power estimation signal and a maximum acceptable power signal;

15 an excess power correction generator that utilizes the scaling factor and the first delayed signal to generate an excess power correction signal;

a filtering apparatus that filters the excess power correction signal to generate a filtered excess power
20 correction signal; and

an excess power removal apparatus that utilizes the filtered excess power correction signal and the second delayed signal to generate the output signal.

25 2. A peak power regulator according to claim 1, wherein the scaling factor is equal to one if the scaling factor generator determines the overall input power estimation signal is less than or equal to the maximum acceptable power signal; and

30 wherein the scaling factor is equal to the maximum acceptable power signal divided by the overall input power

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estimation signal if the scaling factor generator determines the overall input power estimation signal is greater than the maximum acceptable power signal.

5 3. A peak power regulator according to claim 1,
wherein the excess power correction generator comprises a
multiplier used to multiply the first delayed signal by a
factor equal to one minus the scaling factor in order to
generate the excess power correction signal and the filtering
10 apparatus comprises a lowpass filter used to filter the
excess power correction signal.

4. A peak power regulator according to claim 1,
wherein the excess power removal apparatus comprises a
15 differential adder that subtracts the filtered excess power
correction signal from the second delayed signal to generate
the output signal.

5. A peak power regulator according to claim 1,
20 wherein the scaling factor generator comprises a first stage
apparatus and a second stage apparatus;

wherein the output of the first stage apparatus is equal to one if the first stage apparatus determines the overall input power estimation signal is less than or equal to the maximum acceptable power signal;

wherein the output of the first stage apparatus is equal to the maximum acceptable power signal divided by the overall input power estimation signal if the first stage apparatus determines the overall input power estimation signal is greater than the maximum acceptable power signal; and

wherein the output of the second stage apparatus is the scaling factor, the scaling factor being equal to the output from the first stage apparatus divided by a root mean squared (RMS) output from the first stage apparatus over a
5 predetermined period.

6. A peak power regulator according to claim 1, input with in-phase and quadrature baseband input signals, that outputs in-phase and quadrature baseband output signals;

10 wherein the first and second delay apparatus generate first and second delayed in-phase and quadrature baseband signals;

15 wherein the power estimation apparatus generates the overall input power estimation signal corresponding to the baseband input signals with use of the baseband input signals;

20 wherein the excess power correction generator utilizes the scaling factor and the first delayed in-phase and quadrature baseband signals to generate in-phase and quadrature excess power correction signals;

25 wherein the filtering apparatus filters the in-phase and quadrature excess power correction signals to generate filtered in-phase and quadrature excess power correction signals; and

30 wherein the excess power removal apparatus utilizes the filtered in-phase and quadrature excess power correction signals and the second delayed in-phase and quadrature baseband signals to generate the in-phase and quadrature baseband output signals.

7. A peak power regulator according to claim 6,

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wherein the power estimation apparatus comprises:

an in-phase baseband square device, input with the in-phase baseband input signal, that outputs a squared in-phase baseband signal;

5 a quadrature baseband square device, input with the quadrature baseband input signal, that outputs a squared quadrature baseband signal; and

an adder, input with the squared in-phase and quadrature baseband signals, that generates the overall input power estimation signal by summing the squared in-phase and quadrature baseband signals;

wherein the overall input power estimation signal corresponds to an overall input power level squared for the combined in-phase and quadrature baseband input signals and the maximum acceptable power signal corresponds to a maximum acceptable power level squared.

8. A peak power regulator according to claim 6,
wherein the scaling factor is equal to one if the scaling
factor generator determines the overall input power
estimation signal is less than or equal to the maximum
acceptable power signal; and

wherein the scaling factor is equal to the maximum acceptable power signal divided by the overall input power. estimation signal if the scaling factor generator determines the overall input power estimation signal is greater than the maximum acceptable power signal.

9. A peak power regulator according to claim 6,
30 wherein the excess power correction generator comprises two
multipliers used to multiply both the first delayed in-phase

and quadrature baseband signals by a factor equal to one minus the scaling factor to generate the in-phase and quadrature excess power correction signals and the filtering apparatus comprises two lowpass filters used to filter the in-phase and quadrature excess power correction signals.

10. A peak power regulator according to claim 6, wherein the excess power removal apparatus comprises two differential adders that subtract the filtered in-phase and quadrature excess power correction signals from the second delayed in-phase and quadrature baseband signals to generate the in-phase and quadrature baseband output signals.

11. A peak power regulator according to claim 6, wherein the scaling factor generator comprises a first stage apparatus and a second stage apparatus;

wherein the output of the first stage apparatus is equal to one if the first stage apparatus determines the overall input power estimation signal is less than or equal to the maximum acceptable power signal;

wherein the output of the first stage apparatus is equal to the maximum acceptable power signal divided by the overall input power estimation signal if the first stage apparatus determines the overall input power estimation signal is greater than the maximum acceptable power signal; and

wherein the output of the second stage apparatus is the scaling factor, the scaling factor being equal to the output from the first stage apparatus divided by a root mean squared (RMS) output from the first stage apparatus over a predetermined period.

12. A CDMA transmitter comprising:

a data source coupled in series with a channel encoder and spreader, and a baseband pulse shaping filter;

5 a peak power regulator according to claim 6 input with the outputs from the baseband pulse shaping filter, the outputs from the baseband pulse shaping filter corresponding to the in-phase and quadrature baseband input signals; and

10 a quadrature modulator, input with the in-phase and quadrature baseband output signals, coupled in series with an up-converter, a power amplifier, a radio frequency filter, and an antenna.

13. A CDMA transmitter comprising:

15 a data source coupled in series with a channel encoder and spreader, and a baseband pulse shaping filter;

20 a plurality of peak power regulators according to claim 6 coupled in series, a first peak power regulator input with the outputs from the baseband pulse shaping filter, the outputs from the baseband pulse shaping filter corresponding to the in-phase and quadrature baseband input signals; and

25 a quadrature modulator, input with the in-phase and quadrature baseband output signals from a last peak power regulator, coupled in series with an up-converter, a power amplifier, a radio frequency filter, and an antenna.

14. A CDMA transmitter comprising:

30 a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, and a plurality of baseband pulse shaping filters that each output in-phase and quadrature baseband signals;

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a multi-carrier combiner that combines the in-phase and quadrature baseband signals received from the baseband pulse shaping filters to generate the in-phase and quadrature baseband input signals;

- 5 a peak power regulator according to claim 6; and
a quadrature modulator, input with the in-phase and quadrature baseband output signals, coupled in series with an up-converter, a power amplifier, a radio frequency filter, and an antenna.

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15. A CDMA transmitter according to claim 14, wherein the multi-carrier combiner comprises:

at least one mixing device, input with the in-phase and quadrature baseband signals from one of the baseband pulse shaping filters, that outputs a pair of mixed in-phase and quadrature baseband signals;

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an in-phase adder, input with the mixed in-phase baseband signal and at least one in-phase baseband signal from another of the baseband pulse shaping filters, that outputs the in-phase baseband input signal; and

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a quadrature adder, input with the mixed quadrature baseband signal and at least one quadrature baseband signal from the other of the baseband pulse shaping filters, that outputs the quadrature baseband input signal.

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16. A CDMA transmitter according to claim 14, wherein the multi-carrier combiner comprises:

a plurality of mixing devices in which each mixing device is input with one pair of in-phase and quadrature baseband signals from one of the baseband pulse shaping filters and outputs a pair of mixed in-phase and quadrature

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baseband signals;

an in-phase adder, input with the mixed in-phase baseband signals, that outputs the in-phase baseband input signal; and

5 a quadrature adder, input with the mixed quadrature baseband signals, that outputs the quadrature baseband input signals.

17. A CDMA transmitter comprising:

10 a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, and a plurality of baseband pulse shaping filters;

15 a multi-carrier combiner that combines the outputs from the baseband pulse shaping filters to generate the in-phase and quadrature baseband input signals;

a plurality of peak power regulators according to claim 6 coupled in series, a first peak power regulator input with the in-phase and quadrature baseband input signals output from the multi-carrier combiner;

20 a quadrature modulator, input with the in-phase and quadrature baseband output signals from a last peak power regulator, coupled in series with an up-converter, a power amplifier, a radio frequency filter, and an antenna.

25 18. A CDMA transmitter according to claim 17, wherein the multi-carrier combiner comprises:

at least one mixing device, input with the in-phase and quadrature baseband signals from one of the baseband pulse shaping filters, that outputs a pair of mixed in-phase and quadrature baseband signals;

30 an in-phase adder, input with the mixed in-phase

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baseband signal and at least one in-phase baseband signal from another of the baseband pulse shaping filters, that outputs the in-phase baseband input signal; and

5 a quadrature adder, input with the mixed quadrature baseband signal and at least one quadrature baseband signal from the other of the baseband pulse shaping filters, that outputs the quadrature baseband input signal.

19. A CDMA transmitter according to claim 17, wherein
10 the multi-carrier combiner comprises:

a plurality of mixing devices in which each mixing device is input with one pair of in-phase and quadrature baseband signals from one of the baseband pulse shaping filters and outputs a pair of mixed in-phase and quadrature baseband signals;

an in-phase adder, input with the mixed in-phase baseband signals, that outputs the in-phase baseband input signal; and

20 a quadrature adder, input with the mixed quadrature
baseband signals, that outputs the quadrature baseband input
signals.

20. A peak power regulator according to claim 1, input
with a plurality of pairs of in-phase and quadrature baseband
25 input signals, that outputs a plurality of pairs of in-phase
and quadrature baseband output signals;

wherein the first and second delay apparatus generate a plurality of pairs of first and second delayed in-phase and quadrature baseband signals;

wherein the power estimation apparatus generates the overall input power estimation signal corresponding to

the pairs of baseband input signals with use of the pairs of baseband input signals;

wherein the excess power correction generator utilizes the scaling factor and the pairs of first delayed in-phase and quadrature baseband signals to generate a plurality of pairs of in-phase and quadrature excess power correction signals;

wherein the filtering apparatus filters the in-phase and quadrature excess power correction signals to generate filtered in-phase and quadrature excess power correction signals; and

wherein the excess power removal apparatus utilizes the filtered in-phase and quadrature excess power correction signals and the second delayed in-phase and quadrature baseband signals to generate the in-phase and quadrature baseband output signals.

21. A peak power regulator according to claim 20, wherein the power estimation apparatus comprises:

20 a plurality of in-phase baseband square devices,
each input with one of the in-phase baseband input signals,
that output a plurality of squared in-phase baseband signals;

25 a plurality of quadrature baseband square devices,
each input with one of the quadrature baseband input signals,
that output a plurality of squared quadrature baseband
signals;

a plurality of first adders, each input with one of the pairs of squared in-phase and quadrature baseband signals, that sums each pair of squared in-phase and quadrature baseband signals to generate a plurality of first sums;

a plurality of square root devices, each input with one of the first sums, that square root the first sums to generate a plurality of baseband pair input power estimation signals; and

5 a second adder, input with the baseband pair input power estimation signals, that sums the baseband pair input power estimation signals to generate the overall input power estimation signal.

10 22. A peak power regulator according to claim 20,
wherein the power estimation apparatus comprises:

at least one mixing device, input with one pair of in-phase and quadrature baseband input signals, that outputs a pair of mixed in-phase and quadrature baseband signals;

15 an in-phase adder, input with the mixed in-phase
baseband signal and at least one in-phase baseband input
signal, that outputs an in-phase sum;

20 a quadrature adder, input with the mixed quadrature baseband signal and at least one quadrature baseband input signal, that outputs a quadrature sum;

in-phase and quadrature square devices, input with the in-phase and quadrature sums respectively, that outputs squared in-phase and quadrature sums respectively;

25 a final adder, input with the squared in-phase and quadrature sums, that generates the overall input power estimation signal.

23. A peak power regulator according to claim 20, wherein the power estimation apparatus comprises:

30 at least one mixing device, input with one pair of in-phase and quadrature baseband input signals, that outputs

a pair of mixed in-phase and quadrature baseband signals;
an in-phase adder, input with the mixed in-phase
baseband signal and at least one in-phase baseband input
signal, that outputs an in-phase sum;

5 a quadrature adder, input with the mixed quadrature baseband signal and at least one quadrature baseband input signal, that outputs a quadrature sum;

in-phase and quadrature square devices, input with
the in-phase and quadrature sums respectively, that outputs
10 squared in-phase and quadrature sums respectively;

a final adder, input with the squared in-phase and quadrature sums, that outputs a final sum; and

15 a square root device, input with the final sum,
that square roots the final sum to generate the overall input
power estimation signal.

24. A peak power regulator according to claim 20, wherein the power estimation apparatus comprises:

20 a plurality of mixing devices in which each mixing device, input with one pair of in-phase and quadrature baseband input signals, outputs a pair of mixed in-phase and quadrature baseband signals;

an in-phase adder, input with the mixed in-phase baseband signals, that outputs an in-phase sum;

25 a quadrature adder, input with the mixed quadrature
baseband signals, that outputs a quadrature sum;

in-phase and quadrature square devices, input with the in-phase and quadrature sums respectively, that outputs squared in-phase and quadrature sums respectively;

30 a final adder, input with the squared in-phase and
quadrature sums, that generates the overall input power

estimation signal.

25. A peak power regulator according to claim 20, wherein the power estimation apparatus comprises:

5 a plurality of mixing devices in which each mixing device, input with one pair of in-phase and quadrature baseband input signals, outputs a pair of mixed in-phase and quadrature baseband signals;

an in-phase adder, input with the mixed in-phase
10 baseband signals, that outputs an in-phase sum;

a quadrature adder, input with the mixed quadrature baseband signals, that outputs a quadrature sum;

in-phase and quadrature square devices, input with the in-phase and quadrature sums respectively, that outputs squared in-phase and quadrature sums respectively;

a final adder, input with the squared in-phase and quadrature sums, that outputs a final sum; and

a square root device, input with the final sum,
that square roots the final sum to generate the overall input
20 power estimation signal.

26. A peak power regulator according to claim 20, wherein the scaling factor is equal to one if the scaling factor generator determines the overall input power estimation signal is less than or equal to the maximum acceptable power signal; and

wherein the scaling factor is equal to the maximum acceptable power signal divided by the overall input power estimation signal if the scaling factor generator determines the overall input power estimation signal is greater than the maximum acceptable power signal.

27. A peak power regulator according to claim 20,
wherein the excess power correction generator comprises a
plurality of pairs of multipliers used to multiply each first
5 delayed in-phase and quadrature baseband signal by a factor
equal to one minus the scaling factor to generate the in-
phase and quadrature excess power correction signals and the
filtering apparatus comprises a plurality of lowpass filters
used to filter the in-phase and quadrature excess power
10 correction signals.

28. A peak power regulator according to claim 20,
wherein the excess power removal apparatus comprises a
plurality of differential adders that subtract the filtered
15 in-phase and quadrature excess power correction signals from
the corresponding second delayed in-phase and quadrature
baseband signals to generate the in-phase and quadrature
baseband output signals.

29. A peak power regulator according to claim 20,
wherein the scaling factor generator comprises a first stage
apparatus and a second stage apparatus;

wherein the output of the first stage apparatus is
equal to one if the first stage apparatus determines the
25 overall input power estimation signal is less than or equal
to the maximum acceptable power signal;

wherein the output of the first stage apparatus is
equal to the maximum acceptable power signal divided by the
overall input power estimation signal if the first stage
30 apparatus determines the overall input power estimation
signal is greater than the maximum acceptable power signal;

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and

wherein the output of the second stage apparatus is the scaling factor, the scaling factor being equal to the output from the first stage apparatus divided by a root mean squared (RMS) output from the first stage apparatus over a predetermined period.

30. A CDMA transmitter comprising:

a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, and a plurality of baseband pulse shaping filters;

a peak power regulator according to claim 20 input with the outputs from the baseband pulse shaping filters, the outputs from each baseband pulse shaping filter corresponding to one of the pairs of in-phase and quadrature baseband input signals;

a plurality of quadrature modulators, each input with one of the pairs of in-phase and quadrature baseband output signals; and

a combiner, that combines the outputs from the quadrature modulators, coupled in series with an up-converter, a multi-carrier power amplifier, a radio frequency filter, and an antenna.

31. A CDMA transmitter comprising:

a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, and a plurality of baseband pulse shaping filters;

a plurality of peak power regulators according to claim 20 coupled in series, a first peak power regulator input with the outputs from the baseband pulse shaping

filters, the outputs from each baseband pulse shaping filter corresponding to one of the pairs of in-phase and quadrature baseband input signals;

a plurality of quadrature modulators, each input
5 with one of the pairs of in-phase and quadrature baseband
output signals from a last peak power regulator; and

a combiner, that combines the outputs from the quadrature modulators, coupled in series with an up-converter, a multi-carrier power amplifier, a radio frequency filter, and an antenna.

32. An envelope magnitude regulator, input with at least one IF input signal, that outputs at least one IF output signal corresponding to the IF input signal, the envelope magnitude regulator comprising:

first and second delay apparatus that generate first and second delayed IF signals corresponding to the IF input signal;

an envelope magnitude estimation apparatus that
20 generates, with use of the IF input signal, an overall input
envelope magnitude estimation signal corresponding to the IF
input signal;

25 a scaling factor generator that generates a scaling
factor with use of the overall input envelope magnitude
estimation signal and a maximum acceptable envelope magnitude
signal;

an excess power correction generator that utilizes the scaling factor and the first delayed IF signal to generate an excess power correction signal;

30 a filtering apparatus that filters the excess power
correction signal to generate a filtered excess power

correction signal; and

an excess power removal apparatus that utilizes the filtered excess power correction signal and the second delayed IF signal to generate the IF output signal.

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33. A CDMA transmitter comprising:

a data source coupled in series with a channel encoder and spreader, a baseband pulse shaping filter, and a quadrature modulators;

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an envelope magnitude regulator according to claim 32 input with the output from the quadrature modulator, the output from the quadrature modulator corresponding to the IF input signal; and

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an up-converter, input with the IF output signal, coupled in series with a power amplifier, a radio frequency filter, and an antenna.

34. A CDMA transmitter comprising:

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a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, a plurality of baseband pulse shaping filters, and a plurality of quadrature modulators;

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a combiner, that combines the outputs from the quadrature modulators;

an envelope magnitude regulator according to claim 32 input with the output from the combiner, the output from the combiner corresponding to the IF input signal; and

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an up-converter, input with the IF output signal, coupled in series with a multi-carrier power amplifier, a radio frequency filter, and an antenna.

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35. An envelope magnitude regulator according to claim
32, input with a plurality of IF input signals, that outputs
a plurality of IF output signals;

wherein the first and second delay apparatus
5 generate a plurality of first and second delayed IF signals;
wherein the envelope magnitude estimation apparatus
generates the overall input envelope magnitude estimation
signal corresponding to the IF input signals with use of the
IF input signals;

10 wherein the excess power correction generator
utilizes the scaling factor and the first delayed IF signals
to generate a plurality of excess power correction IF
signals;

wherein the filtering apparatus filters the excess
15 power correction IF signals to generate filtered excess power
correction IF signals; and

wherein the excess power removal apparatus utilizes the filtered excess power correction signals and the second delayed IF signals to generate the IF output signals.

36. An envelope magnitude regulator according to claim 35, wherein the envelope magnitude estimation apparatus comprises:

an adder, input with the IF input signals, that
25 sums the IF input signals to generate a first sum; and
an envelope detector, input with the first sum,
that generates the overall input envelope magnitude
estimation signal.

30 37. An envelope magnitude regulator according to claim
36, wherein the envelope detector comprises:

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an absolute value device that generates an absolute value IF signal with use of the first sum; and

a maximum value detector, input with the absolute value IF signal, that determines the maximum input value over a predetermined amount of time, this maximum input value corresponding to the overall input envelope magnitude estimation signal.

38. An envelope magnitude regulator according to claim 36, wherein the envelope detector comprises:

an up-sampling and interpolation device that generates an interpolated IF signal with use of the first sum;

an absolute value device that generates an absolute value IF signal with use of the interpolated IF signal; and

a maximum value detector, input with the absolute value IF signal, that determines the maximum input value over a predetermined amount of time, this maximum input value corresponding to the overall input envelope magnitude estimation signal.

39. An envelope magnitude regulator according to claim 35, wherein the scaling factor is equal to one if the scaling factor generator determines the overall input envelope magnitude estimation signal is less than or equal to the maximum acceptable envelope magnitude signal; and

wherein the scaling factor is equal to the maximum acceptable envelope magnitude signal divided by the overall input envelope magnitude estimation signal if the scaling factor generator determines the overall input envelope magnitude estimation signal is greater than the maximum

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acceptable envelope magnitude signal.

40. An envelope magnitude regulator according to claim 35, wherein the excess power correction generator comprises a plurality of multipliers used to multiply each first delayed IF signal by a factor equal to one minus the scaling factor to generate the excess power correction IF signals and the filtering apparatus comprises a plurality of bandpass filters used to filter the excess power correction IF signals.

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41. An envelope magnitude regulator according to claim 35, wherein the excess power removal apparatus comprises a differential adder that subtracts the filtered excess power correction IF signals from the second delayed IF signals to generate the output IF signals.

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42. An envelope magnitude regulator according to claim
35, wherein the scaling factor generator comprises a first
stage apparatus and a second stage apparatus;

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wherein the output of the first stage apparatus is equal to one if the first stage apparatus determines the overall input envelope magnitude estimation signal is less than or equal to the maximum acceptable envelope magnitude signal;

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25 wherein the output of the first stage apparatus is
equal to the maximum acceptable envelope magnitude signal
divided by the overall input envelope magnitude estimation
signal if the first stage apparatus determines the overall
input envelope magnitude estimation signal is greater than
30 the maximum acceptable envelope magnitude signal; and

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wherein the output of the second stage apparatus is

the scaling factor, the scaling factor being equal to the output from the first stage apparatus divided by a root mean squared (RMS) output from the first stage apparatus over a predetermined period.

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43. A CDMA transmitter comprising:

a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, a plurality of baseband pulse shaping filters, and a plurality of quadrature modulators;

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an envelope magnitude regulator according to claim 35 input with the outputs from the quadrature modulators, the output from each quadrature modulator corresponding to one of the IF input signals; and

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a combiner, that combines the IF output signals from the envelope magnitude regulator, coupled in series with an up-converter, a multi-carrier power amplifier, a radio frequency filter, and an antenna.

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44. A CDMA transmitter comprising:

a plurality of data sources coupled in series with a plurality of channel encoder and spreaders, a plurality of baseband pulse shaping filters, and a plurality of quadrature modulators;

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a plurality of envelope magnitude regulators according to claim 35 coupled in series, a first envelope magnitude regulator input with the outputs from the quadrature modulators, the output from each quadrature modulator corresponding to one of the IF input signals; and

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a combiner, that combines the IF output signals from a last envelope magnitude regulator, coupled in series

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with an up-converter, a multi-carrier power amplifier, a radio frequency filter, and an antenna.

45. In a peak power regulator, input with at least one input signal, that outputs at least one output signal corresponding to the input signal, a method for regulating output power comprising the steps of:

estimating the overall input power level corresponding to the input signal;

10 generating a scaling factor with use of the estimate of the overall input power level and a maximum acceptable input power signal;

delaying the input signal by a first amount;

15 generating an excess power correction signal with use of the scaling factor and the input signal delayed by the first amount;

filtering the excess power correction signal;

delaying the input signal by a second amount larger than the first amount; and

20 generating the output signal with use of the input signal delayed by the second amount and the filtered excess power correction signal.

46. A peak power regulator, input with at least one input signal, that outputs at least one output signal corresponding to the input signal, the power regulator comprising:

25 first and second delay apparatus that generate first and second delayed signals corresponding to the input signal;

30 a power estimation apparatus that generates, with

